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In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A semiconductor device, comprising:

a capacitor having a bottom electrode, a dielectric layer formed on the bottom electrode, and an upper electrode formed on the dielectric layer, the capacitor being formed on a semiconductor substrate, wherein the bottom electrode, the dielectric layer, and the upper electrode are vertically arranged;

a first insulating layer formed on the semiconductor substrate to cover the capacitor;

a plurality of first contact plugs formed in a plurality of first via holes of the first insulating layer, each of the plurality of first contact plugs being electrically connected to either the bottom electrode or the upper electrode ~~electrodes~~;

a first metal wiring formed on the first insulating layer and connected to the bottom electrode through one of the first contact plugs;

a second insulating layer formed on the first insulating layer;

a second contact plug in the second insulating layer formed on the first insulating layer and connected to the upper electrode through another one of the first contact plugs;

an anti-fuse formed in certain thickness in a second via hole of the second insulating layer and electrically connected to the second contact plug;

a third contact plug filling the second via hole and formed within the anti-fuse, wherein the third contact plug does not directly contact the second insulating layer; and

a second metal wiring formed on the second insulating layer and electrically connected to the third contact plug and the anitfuse.

2. (Original) The semiconductor device of claim 1, wherein the first and second metal wirings are arranged perpendicular to each other.

3. (Currently Amended) A method of manufacturing a semiconductor device, comprising:

forming a capacitor ~~capacitors~~ having a bottom electrode, a dielectric layer formed on the bottom electrode and an upper electrode formed on the dielectric layer on a semiconductor substrate,

wherein the bottom electrode, the dielectric layer, and the upper electrode are vertically arranged;

forming a first insulating layer on the semiconductor substrate to cover the capacitor capacitors;

forming a plurality of first via holes exposing surfaces of the bottom electrode and the upper electrode electrodes by selectively patterning the first insulating layer;

forming a plurality of first contact plugs by filling the first via holes with metal materials;

forming first metal wiring connected to the bottom electrode electrodes through one some of the plurality of first contact plugs and forming a second contact plug plugs connected to the upper electrode electrodes through another one of the other plurality of first contact plugs, on the first insulating layer;

forming a second insulating layer on the first insulating layer;

forming a plurality of second via hole holes exposing a surface surfaces of the second contact plugs plug by selectively patterning the second insulating layer;

successively depositing first and second metal layers on the second insulating layer including the second via hole holes;

forming an anti-fuse anti-fuses in the second via hole holes and a third contact plug plugs within the anti-fuse anti-fuses by planarizing the first and second metal layers with the second insulating layer; and

forming second metal wiring electrically connected to the anti-fuse anti-fuses and the third contact plug plugs, on the second insulating layer.